What is claim d is:

1. An array substrate device for use in an IPS LCD device, comprising:

a gate line disposed in a transverse direction on a substrate;

a data line disposed in a longitudinal direction perpendicularly crossing the gate line, the data line defining a pixel region with the gate line;

a common line disposed in a transverse direction adjacent to the gate line on the substrate;

a thin film transistor adjacent to a crossing portion of the gate and data lines, the thin film transistor including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a plurality of common electrodes in the pixel region on the substrate, one ends of the plurality of common electrodes coupled with the common line;

a gate insulation layer covering the gate line, the gate electrode, the common line and the plurality of common electrodes;

a passivation layer covering the data line, the source electrode and the drain electrode, the passivation layer having a drain contact hole exposing the drain electrode;

a plurality of pixel electrodes in the pixel region on the substrate, wherein the plurality of pixel electrodes and common electrodes are arranged in an alternating manner and a pair of pixel and common electrodes define a sub-pixel region with a predetermined interval therebetween;

a first pixel connecting line disposed on the passivation layer over the common line and coupled with one ends of the plurality of pixel electrodes;

first slanted slopes at corners where the common electrodes meet the common line in upper portions of one of the even- and odd-numbered sub-pixel regions; and

second slanted slopes at corners where the pixel electrodes meet the first pixel connecting line in the upper portions of one of the even- and odd-numbered sub-pixel regions;

wherein each of the first slanted slopes and each of the second slanted slopes cross each other.

2. The array substrate device of claim 1, wherein the first slanted slopes have a first obtuse angle with respect to the common electrodes.

3. The array substrate device of claim 2, wherein the first obtuse angle ranges from about 100 to 150 degrees.

4. The array substrate device of claim 1, wherein the second slanted slopes have a second obtuse angle with respect to the pixel electrodes.

5. The array substrate device of claim 4, wherein the second obtuse angle ranges from about 100 to 150 degrees.

6. The array substrate device of claim 1, wherein the plurality of pixel electrodes and the pixel connecting line are electrically connected with the drain electrode of the thin film transistor.

7. The array substrate device of claim 1, wherein the plurality of common electrodes and the plurality of pixel electrodes are parallel with the data line.

8. The array substrate device of claim 1, further comprising:

a common connecting line on the substrate, the common connecting line connected with the other ends of the plurality of common electrodes in an opposite direction of the common line;

third slanted slopes at corners where the common electrodes meet the common connecting line in lower portions of one of the even- and odd-numbered sub-pixel regions;

a second pixel connecting line on the passivation layer over the common connecting line, the second pixel connecting line connected with the other ends of the plurality of pixel electrodes in an opposite direction of the first pixel connecting line; and

fourth slanted slopes at corners where the pixel electrodes meet the second pixel connecting line in the lower portions of one of the even- and odd-numbered sub-pixel regions.

9. The array substrate device of claim 8, wherein each of the third slanted slopes and each of the fourth slanted slopes cross each other.

10. The array substrate device of claim 8, wherein the third slanted slopes have a third obtuse angle with respect to the common electrodes.

11. The array substrate device of claim 10, wherein the third obtuse angle ranges from about 100 to 150 degrees.

12. The array substrate device of claim 8, wherein the fourth slanted slopes have a fourth obtuse angle with respect to the pixel electrodes.

13. The array substrate device of claim 12, wherein the fourth obtuse angle ranges from about 100 to 150 degrees.

14. The array substrate device of claim 8, wherein the first and second slanted portions are disposed in the upper portions of the even-numbered sub-pixel regions, and the third and fourth slanted portions

are disposed in the lower portions of the odd-numbered sub-pixel regions.

15. The array substrate device of claim 8, wherein the first and second slanted portions are disposed in the upper portions of the odd-numbered sub-pixel regions, and the third and fourth slanted portions are disposed in the lower portions of the even-numbered sub-pixel regions.

16. An array substrate device for use in an IPS LCD device, comprising:

a common line disposed in a transverse direction adjacent to a gate line on a substrate;

a plurality of common electrodes in a pixel region on the substrate, one ends of the plurality of common electrodes coupled with the common line;

a plurality of pixel electrodes in the pixel region on the substrate, wherein the plurality of pixel electrodes and common electrodes are arranged in an alternating manner and a pair of pixel and common electrodes define a sub-pixel region with a predetermined interval therebetween;

a first pixel connecting line disposed over the common line and coupled with one ends of the plurality of pixel electrodes;

first slanted slopes at corners where the common electrodes meet the common line in upper portions of one of the even- and odd-numbered sub-pixel regions; and

second slanted slopes at corners where the pixel electrodes meet the first pixel connecting line in the upper portions of one of the even- and odd-numbered sub-pixel regions;

wherein each of the first slanted slopes and each of the second slanted slopes cross each other.

17. The array substrate device of claim 16, wherein the first slanted slopes have a first obtuse angle with respect to the common electrodes, and the second slanted slopes have a second obtuse angle with respect to the pixel electrodes.

18. The array substrate device of claim 16, further comprising:

a common connecting line on the substrate, the common connecting line connected with the other ends of the plurality of common electrodes in an opposite direction of the common line;

third slanted slopes at corners where the common electrodes meet the common connecting line in lower portions of one of the even- and odd-numbered sub-pixel regions;

a second pixel connecting line over the common connecting line, the second pixel connecting line connected with the other ends of the plurality of pixel electrodes in an opposite direction of the first pixel connecting line; and

fourth slanted slopes at corners where the pixel electrodes meet the second pixel connecting line in the lower portions of one of the even- and odd-numbered sub-pixel regions.

19. The array substrate device of claim 18, wherein the first and second slanted portions are disposed in the upper portions of the even-numbered sub-pixel regions, and the third and fourth slanted portions are disposed in the lower portions of the odd-numbered sub-pixel regions.

20. The array substrate device of claim 18, wherein the first and second slanted portions are disposed in the upper portions of the odd-numbered sub-pixel regions, and the third and fourth slanted portions

are disposed in the lower portions of the even-numbered sub-pixel regions.